Code No.: **30403/40403** **MR13/ MR14**

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

(Affiliated to JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD)
Gundlapochampally (H), Maisammaguda (V), Medchal (M), Medchal-Malkajgiri (Dist), Hyderabad

II B.TECH II SEMESTER SUPPLEMENTARY EXAMINATIONS, DECEMBER-2018

Subject: **SWITCHING THEORY AND LOGIC DESIGN**

Branch: **EEE**

Time: 3 hours **Max. Marks: 75**

PART – A

I. Answer ALL questions of the following **5x1Mark=5 Marks**

1. Convert the following binary numbers to Gray code a) 111100 b) 101001
2. Simplify the Boolean function x'yz + x'yz' + xy'z' + xy'z without using K-map
3. What is Flip Flop?
4. How many numbers of flipflops are required to implement mod-13 counter?
5. Write the expression for next state of mealy model machine

II. Answer ALL questions of the following **10x2Mark=20 Marks**

1. Express the Decimal digits 0-9 in BCD, 2421, 8-4-2-1 and excess-3 codes
2. Determine the complement of theF = $A\bar{B}C + \bar{A}BD$.
3. Simplify the following Boolean expression using K-Map. F = $\sum(0,2,4,6)$
4. What is comparator? Write the output expressions of 2 bit comparator
5. Write a short note on master slave J-K flip-flop
6. Draw the k-map for next state of D-Flip flop
7. Design Mod3 up counter using D-flip-flop
8. Distinguish between synchronous and asynchronous circuits.
9. State 'State equivalence theorem'
10. Draw Mealy sequential circuit model.

PART-B

Answer ALL questions of the following **5x10 Marks= 50Marks**

1. a) Develop a Gray code for $(84)_{10}$ and $(35)_{10}$ and convert the same to Hex sequence [6M]
   b) Explain different error detecting codes [4M]

OR

2. Draw the logic symbol and construct the truth table for each of the following gates.
   a) Three input AND gate b) Three input NAND gate c) three input OR gate
   d) Three input NOR gate e) Three input EX.OR gate.

3. Design a 4-bit binary comparator.

OR

4. a) Determine the canonical POS and SOP form of $T(x,y,z)=x^1(y^1+z^1)$ [4M]

   b) Reduce the following Boolean expression using theorems and identities

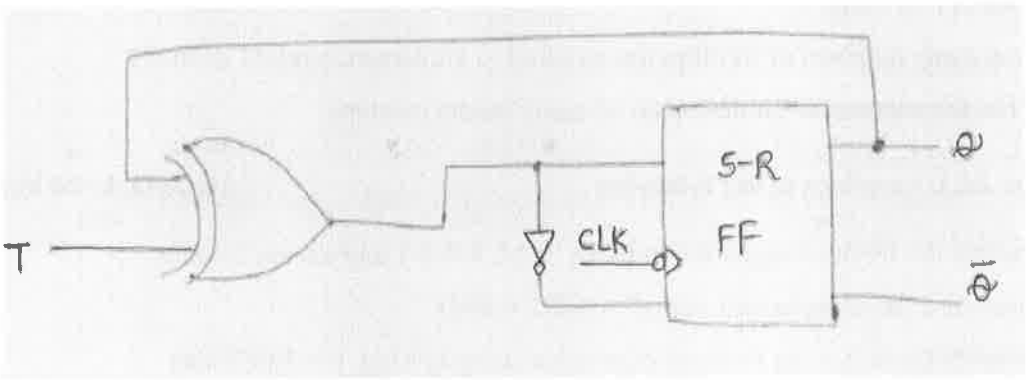
   $F=AB+C\bar{D}B+\bar{A}C\bar{D}$ [6M]

5. Draw the timing diagrams of a) T Flip- Flop b) D Flip Flop.

OR

6. a) Classify the required circuits into synchronous, asynchronous, clock mode, pulse mode with suitable examples.

   b) Prepare the truth table for the following circuit and show that it acts as a T-flip flop.



7. Design a counter with the following binary sequence: 0, 1, 3, 7, 6, 4 and repeat. Use JK flip-flops

OR

8. a) Design a BCD counter using JK flip flops [6M]

   b) What are the design aspects of synchronous sequential finite state machines? [4M]

9. Draw the state diagram for full adder and convert it to ASM chart and realize the above using JK flip flops and gates.

OR

10. Design a control logic through ASM chart for the sequence detector which detects 1100 and resets flip flop F to 0 and flip flop E to 1. The patterns come from 4 bit counter A

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II B.TECH II SEMESTER SUPPLEMENTARY EXAMINATIONS, DECEMBER-2018

Subject: : **Electrical Machines-II**

Branch: **EEE**

Time: 3 hours **Max. Marks: 75**

PART – A

I. Answer ALL questions of the following **5x1Mark=5 Marks**

1. Define Transformer?
2. Which type of connection is commonly used for large low voltage transformer
3. What is the speed of rotor mmf of a 3-ϕ induction motor w.r.t. its stator mmf
4. What is the cheapest method of starting a 3-ϕ induction motor
5. How can the direction of a capacitor-run motor be reversed?

II. Answer ALL questions of the following **10x2Mark=20 Marks**

1. What are the functions of a Transformer?
2. What is an ideal transformer?draw its no-load phasor diagram.
3. Write a short notes on scott connection of 3-ϕ transformer
4. Explain the advantage of using a tertiary winding in a bank of star-star transformers.
5. List the difference between squirrel cage rotor and slip ring rotor.
6. How the direction of rotation of a 3-ϕ induction motor can be reversed?
7. Why starter is necessary for the induction motors?
8. State various methods of speed control of three-phase induction motor.
9. What is meant by split-phase method of motor starting?
10. Name the two theories regarding single phase induction motor.

PART-B

Answer ALL questions of the following **5x10 Marks= 50Marks**

1. a. Draw a no load phasor diagram of a transformer and explain

   b. A 250 kVA single phase transformer has iron loss of 1.8 kW. The full-load copper loss of 2000Watts. Calculate efficiency at full load, 0.8 lagging power factor

(OR)

2. a. Derive condition for maximum efficiency
   b. A 460 / 230 V, 3KVA transformer gave the following results.
   O.C test : 230V ,2A 100W
   S.C test: 15V ,13A, 120W
   Determine the regulation at full load 0.8 p.f lagging

3. What is "on load tap" changing ?explain

(OR)

4. Explain the constructional details of a 3-ϕ transformer, with diagrams
5. Draw the circle diagram for a 20Hp,50Hz,3-ϕ star connected induction motor with the following data

   No load test:400V,9A,0.2 p.f lagging

   Blocked rotor test:200V,50A,0.4 p.f lagging

   Determine line current and efficiency for full load condition from the circle diagram

(OR)

6. Explain the working of following starters with the help of neat circuit diagram

   a. direct on line starter

   b. star-delta starter

7. A 60KW,400V,3-ϕ,6 pole ,50Hz wound rotor induction motor has a full load slip of 0.04 when operating at rated voltage and frequency with rotor winding short slip rings. The slip at maximum torque is 0.2.stator resistance and rotational losses are neglected. Determine i)the maximum torque ii)full load rotor ohmic losses

(OR)

8. Sketch and explain the typical torque-slip characteristics of **3-ϕ induction motor.**
9. Explain why a 1-ϕ induction motor does not self start. Discuss its operation based on double field revolving theory

(OR)

10. Explain with neat diagrams the following types of 1-ϕ induction motors

    a. Split phase induction motor

    b. Capacitor start induction motor

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II B.TECH II SEMESTER SUPPLEMENTARY EXAMINATIONS, DECEMBER-2018

Subject: **ELECTRONIC CIRCUITS**

Branch: **EEE**

Time: 3 hours **Max. Marks: 75**

PART – A

I. Answer ALL questions of the following **5x1Mark=5 Marks**

1. Draw circuit for common gate amplifier.
2. What is heat sink?
3. Why the gain band width product does not get changed by feedback?
4. Define rise time.
5. Which multi vibrator would function as a time delay unit?

II. Answer ALL questions of the following **10x2Mark=20 Marks**

1. Discuss small signal JFET model
2. What are the various-h-parameters for a CE transistor? Write the equations?
3. What are the power considerations in class B amplifiers?
4. Explain class A power amplifier? What is the efficiency of it?
5. Explain working of sine wave feedback oscillator.
6. Define loop gain in wien bridge oscillator with equation.
7. Why RC low pass circuit is called as Integrator?
8. Explain saturation & cut off region? Draw the characteristics of a transistor?
9. Draw Schmitt trigger circuit.
10. Define monostable multi-vibrator? Write the advantages of it.

PART-B

Answer ALL questions of the following **5x10 Marks= 50Marks**

1. a) Evaluate the equations for voltage gain , current gain, input impedance and output impedance for a BJT using low frequency h-parameter model for CC configuration.

   b) Classify the amplifier circuits based on frequency range, type of coupling, power delivered and signal handled.

   OR

2. a) The h-parameters of CE amplifier with RS=1K, RL=10K, hie = 1.1K, $h_{re}=2.5X10^{-4}$, h_{fe} = 50 and h_{oe} = 24μA/V. Find out current and voltage gains with and without source resistance, input and output impedances.

   b) Explain the operation of common Drain FET amplifier.

3. a) Evaluate the expression for maximum conversion efficiency for a simple series fed Class A power amplifier. What are the drawbacks of transformer coupled power amplifiers?

   b) Calculate the ac power delivered to the load of RL = 2KΩ for a single transistor operates as an ideal class B power amplifier, if dc current drawn from the supply is 25mA

OR

4. Draw the circuit of a series fed class A power amplifier and analyze it for its efficiency and power dissipation and proves that maximum efficiency is 25%

5. a) Sketch the block diagram of a feedback amplifier and derive the expressions for gain (1) with positive feedback and (2) with negative feedback. State the advantages of negative feedback.

   b) We have an amplifier of 60dB gain. It has an output impedance Z0 = 10KΩ. It is required to modify its output impedance to 500Ω by applying negative feedback factor. Calculate the value of the feedback factor. Also find the percentage change in the overall gain, for 10% change in the gain of the amplifier without feedback.

OR

6. a) Show that for voltage shunt feedback amplifier transfer gain, Ri and Ro are decreased by a factor (1+Aβ) with feedback.

   b) An amplifier with open loop voltage gain AV = 1000±100 is available. It is necessary to have an amplifier whose voltage gain varies by no more than ±0.1 percent. i. Estimate the reverse transmission factor β of the feedback network used. ii. Estimate the gain with feedback.

7. a) Explain transistor clipping circuit.

   b) Discuss clamping circuit theorem.

OR

8. a) Draw a circuit, to transmit that part of a sine wave which lies between -3V and +6V

   b) Design a diode clamper to restore the positive peaks of 1Khz input signal to a voltage level equal to 5V. assume the voltage drop across diode as 0.7V

9. a) With the help of neat circuit diagram and waveforms, explain the working of an astable multivibrator.

   b) Theselfbiasedbistablemultivibrator uses silicon transistors with h_{FE}(min) =20. The junction voltages and Icbo may be neglected. Design the circuit subject to the condition Vcc=18V, R1= R2, Ic(max)= 10mA. The base current of ON transistor is twicw the minimum base current and V_{BE} of the OFF transistor is equal to -1V

OR

10. Design a Schmitt trigger circuit for the following specifications: Vcc =12V, UTP = 6V, LTP = 4V, IC(max) = 1mA, h_{fe}=30. Assume necessary data

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II B.TECH II SEMESTER SUPPLEMENTARY EXAMINATIONS, DECEMBER-2018

Subject: **NETWORK THEORY**

Branch: **EEE**

Time: 3 hours **Max. Marks: 75**

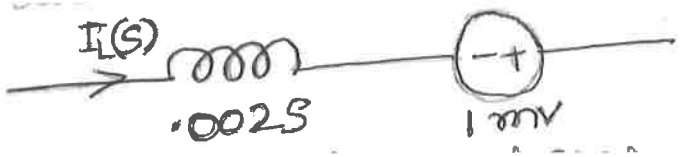
PART – A

I. Answer ALL questions of the following **5x1Mark=5 Marks**

1. What is a balanced load in 3-Φ power systems?
2. What is time constant for an RC series circuit? Mention unit.
3. What is a transfer function?
4. What is a Port?
5. What is attenuation? Mention its unit.

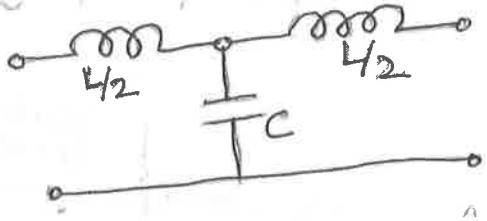
II. Answer ALL questions of the following **10x2Mark=20 Marks**

1. Phase voltage of a circuit is $10\angle 15°$ volts and phase current of the same circuit is $2\angle -45°$ AMP. Find the active & reactive powers.
2. If the total power measured in two wattmeter method is 1000W and power factor is 0.5. Find the reading of each wattmeter.
3. 2 mH inductor with some initial current is represented as shown



Find the value of initial current.

4. If the Laplace transform of voltage across a capacitor of value 0.5F is $V_c(S) = \frac{1}{S^2+1}$ find the value of current through capacitor at t=0+
5. Obtain the pole-zero location for the function $T(S) = \frac{(2S+4)(S+4)}{S(S+1)(S+3)}$ and plot them on S-Plane
6. Find the response with e^{-2t} as input to the transfer function $H(S) = \frac{V_2(S)}{V_1(S)} = \frac{1}{S+3}$
7. The Z- parameters of a two-port network are $Z_{11}=10\Omega$, $Z_{22}=20\Omega$and $Z_{12} = Z_{21} = 5\Omega$ Find its equivalent T-network.
8. T-parametrs of a two pot network are represented as follows:
   $V_1 = {}^4/_3 V_2 - {}^{11}/_3 I_2$
   $I_1 = CV_2 - {}^5/_3 I_2$
   Find 'C' if the network given is reciprocal.
9. Design a lowpass filter with $R_L = 1\Omega$ and $\omega = 1$ rad/sec. Find the value of L & C .



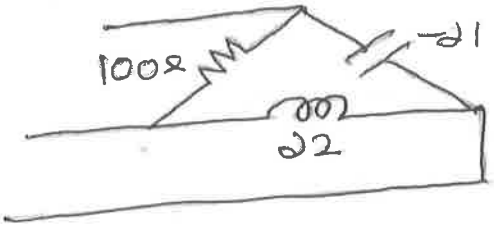
10. A complex wave is given by $i(t) = 10+100 \sin \omega t + 40 \sin 3\omega t$. Determine the rms value of

PART-B

Answer ALL questions of the following **5x10 Marks= 50Marks**

1. a) Each Phase of a balanced star-connected load consists of R=10Ω and C=10μF. Calculate the line currents and total real & reactive power when a symmetrical 400V, 50 Hz, 3ϕ supply is applied.

   b) A set of three equal resistors each of value 'R'Ω connected in 'Y' across the 3ϕ supply in place of unbalanced Δ connected loas as shown in fig. If it consumes the same power, find the value of R.



OR

2. a) A 400V, 50Hz, 3ϕ supply of phase sequence ABC is applied to a delta connected load consisting of 100 ohms resistance between lines A&B, 318 mH inductance between B&C, 31.8μF capacitance between C&A. Determine line currents.

   b) Two wattmeter are used to measure power in a 3-phase three wire load. Determine the total power, power factor and reactive power, if the two wattmeters read

   i) 1000 W each, both positive.

   ii) 1000 W each, but of opposite sign.

3. a) A DC Voltage of 20V is applied in a R-L circuit where R=5Ω and L=10H. Find

   i) the time constant

   ii) energy (maximum) stored

   b) A constant voltage of 100V is applied at t=0 to a series circuit consisting of R=5mΩ and C= 20 mF. Assuming no initial charge on the capacitor. Find the expression for i(t), Voltage across 'R' and 'C'.

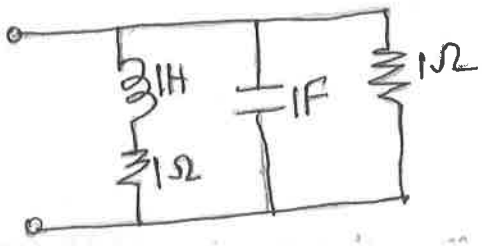
OR

4. a) Ina Series RLC circuit R = 6Ω, L = 2H, C=0.25F and V_s = 2V.

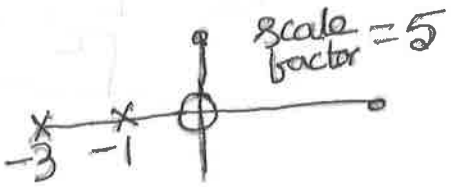
   Find $i(0^+)$, $\frac{di(0^+)}{dt}$, $\frac{d^2i(0^+)}{dt}$

   b) A 50Hz 300V(Peak Value) sinusoidal voltage is applied at t=0 to a series R-L circuit having R=2.5Ω and L= 0.1H. Find an expression for current at any instant.

5. a) Determine the driving point impedance Z_d of the network given. Find the poles and zeroes of the network and locate them in the S-plane.

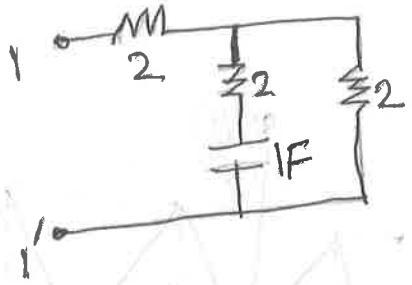


   b) For a fiven Pole-zero diagram find expression for i(t)

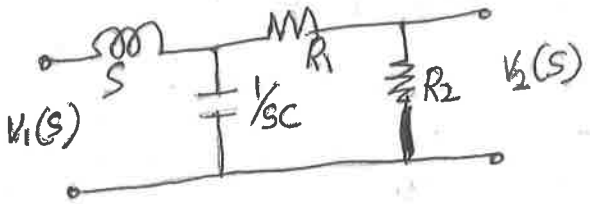


OR

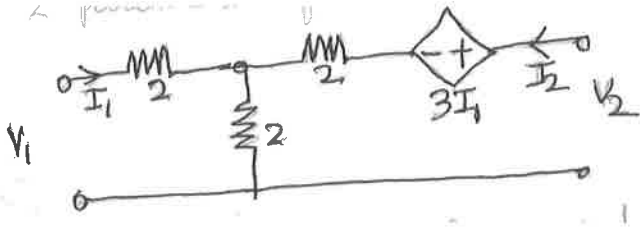
6. a) For a given circuit the voltage source connected at 1-1. The response is the input current. Obtain the network function.



b) The voltage transfer function shown is given by $\frac{0.2}{S^2+3S+2}$. Find the value of parameters.



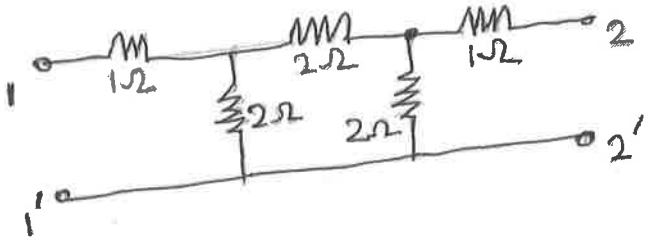
7. a) Find 'Z' parameters of the network shown



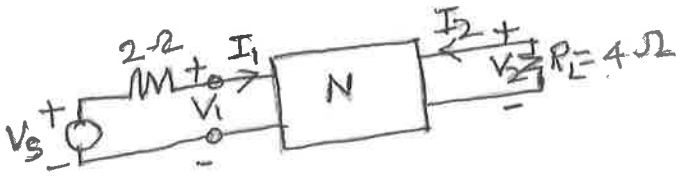
b) A typical two-port network is characterized by the equations $2V_1+4I_2=I_1$ and $V_2+6V_1=8I_2$. Determine the values of i) Y_{11} ii) Z_{21} iii) h_{21}

OR

8. a) Prove that the following network is symmetrical and reciprocal.

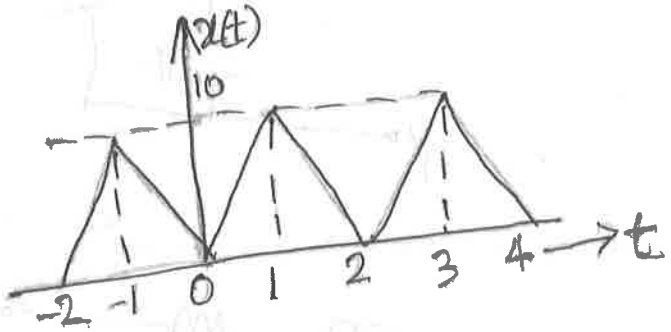


b) The hybrid parameters of the network 'N' are $h_{11}=2\Omega$, $h_{21}= -5$ and $h_{22}= 2\mho$. Find the supply voltage if the power dissipated by load R_L is 25 watts.



9. a) Explain about Fourier theorem.

   b) Find the trigonometric Fourier series for the waveform shown.



OR

10. a) Explain the types of filters based on frequency and draw the ideal characteristics of each filter.

    b) Mention various characteristics of the filter networks.

    c) A signal is attenuated by 30db when the signal strength at the input i.e P_i = 1mW. Find the output power P_0